LP385x 1.5-A Fast Response Ultra-Low Dropout Linear Regulators

1 Features

- Input Supply Voltage: 2.5 V to 7 V
- Ultra-Low Dropout Voltage
- Stable with Selected Ceramic Capacitors
- Low Ground-Pin Current
- Load Regulation of 0.06%
- 10-nA Quiescent Current in Shutdown Mode
- Specified Output Current of 1.5 A DC
- Output Voltage Accuracy ± 1.5%
- $\overline{\text{ERROR}}$ Pin Indicates Output Status
- SENSE Option Improves Load Regulation
- Overtemperature/Overcurrent Protection
- −40°C to 125°C Junction Temperature Range

2 Applications

- Microprocessor Power Supplies
- GTL, GTL+, BTL, and SSTL Bus Terminators
- Power Supplies for DSPs
- SCSI Terminator
- Post Regulators
- High Efficiency Linear Regulators
- Battery Chargers
- Other Battery Powered Applications

3 Description

The LP3852 and LP3855 series of fast ultra-low dropout linear regulators operate from a 2.5-V to 7-V input supply. A wide range of preset output voltage options are available. These ultra-low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. The LP3852 and LP3855 are developed on a CMOS process which allows low quiescent-current operation independent of output load current, typically 4 mA at 1.5-A load current. This CMOS process also allows the LP3852 and LP3855 to operate under extremely low dropout conditions, typically 24 mV at 150-mA load current and 240 mV at 1.5-A load current.

The LP3852 has an $\overline{\text{ERROR}}$ pin; it goes low when the output voltage drops 10% below nominal value. The LP3855 has a SENSE pin to improves regulation at remote loads.

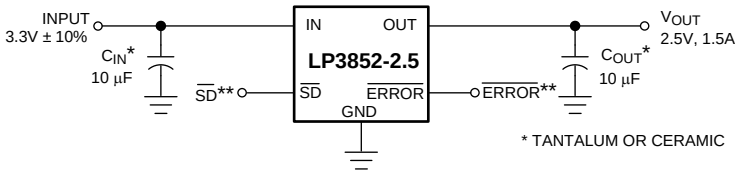
The LP3852 and LP3855 are available with fixed output voltages from 1.8 V to 5 V with a specified accuracy of ±1.5% at room temperature, and ±3% over all conditions (varying line, load, and temperature). Contact Texas Instruments Sales for specific voltage option needs.

Device Information(1)

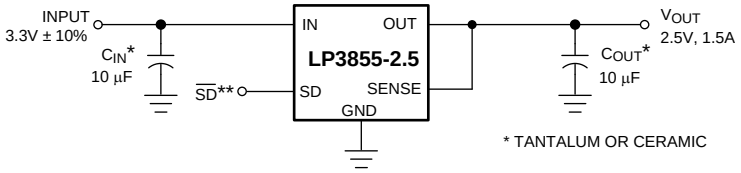
PART NUMBER	PACKAGE	BODY SIZE (NOM)
LP3852 LP3855	SOT (5)	6.50 mm x 3.56 mm
	TO-263 (5)	10.16 mm x 8.42 mm
	TO-220 (5)	14.986 mm x 10.16 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Simplified Schematics



**$\overline{\text{SD}}$ and $\overline{\text{ERROR}}$ pins must be pulled high through a 10-kΩ pull-up resistor. Connect the $\overline{\text{ERROR}}$ pin to ground if this function is not used.



**$\overline{\text{SD}}$ must be pulled high through a 10-kΩ pull-up resistor.

An IMPORTANT NOTICE at the end of this data sheet addresses availability, warranty, changes, use in safety-critical applications, intellectual property matters and other important disclaimers. PRODUCTION DATA.

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5 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision H (December 2014) to Revision I	Page
• Changed pin names to TI nomenclature; correct typos	1
• Changed pin numbers and I/O types to correct errors	4
• Changed *Handling* to *ESD Ratings*	5

Changes from Revision G (April 2013) to Revision H	Page
• Added *Device Information* and *Handling Rating* tables, *Feature Description*, *Device Functional Modes*, *Application and Implementation*, *Power Supply Recommendations*, *Layout*, *Device and Documentation Support*, and *Mechanical, Packaging, and Orderable Information* sections; moved some curves to *Application Curves* section; updated Thermal Values	1

Changes from Revision F (April 2013) to Revision G	Page
• Changed layout of National Data Sheet to TI format	20

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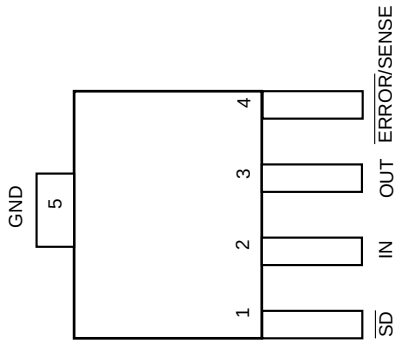
6 Voltage Options[(1)(2)]

DEVICE NUMBER	PACKAGE	VOLTAGE OPTION (V)
LP3852 LP3855	TO-220 (5) DDPAK/TO-263 (5) SOT-223 (5)	1.8
		2.5
		3.3
		5.0

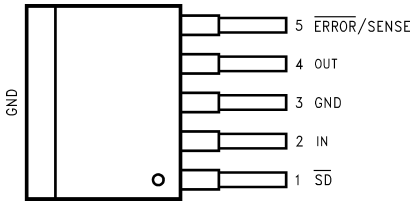
(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available on the Packaging Information page at www.ti.com.

7 Pin Configuration and Functions

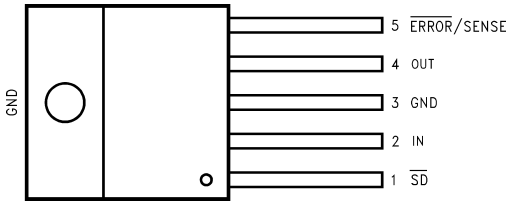
SOT-223 (NDC)
5 Pins
Top View



5 Pins
DDPAK/TO-263 (KTT)
Top View



5 Pins
TO-220 (NDH)
Top View, Bent, Staggered Leads



Pin Functions for SOT-223

PIN			I/O	DESCRIPTION
NAME	LP3852	LP3855		
	NDC	NDC		
$\overline{\text{ERROR}}$	4	N/A	O	$\overline{\text{ERROR}}$ flag
GND	5	5	—	Ground
IN	2	2	I	Input supply
OUT	3	3	O	Output voltage
$\overline{\text{SD}}$	1	1	I	Shutdown
SENSE	N/A	4	I	Remote sense pin

Pin Functions for TO-220 and TO-263

PIN			I/O	DESCRIPTION
NAME	LP3852	LP3855		
	KTT/NDH	KTT/NDH		
$\overline{\text{ERROR}}$	5	N/A	O	$\overline{\text{ERROR}}$ flag
GND	3	3	—	Ground
IN	2	2	I	Input supply
OUT	4	4	O	Output voltage
$\overline{\text{SD}}$	1	1	I	Shutdown
SENSE	N/A	5	I	Remote sense pin

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

	MIN	MAX	UNIT
Lead temperature (soldering, 5 sec.)		260	°C
Power dissipation (2)	Internally limited		
Input supply voltage (survival)	–0.3	7.5	V
Shutdown input voltage (survival)	–0.3	7.5	
Output voltage (survival) (3), (4)	–0.3	6	
I_{OUT} (survival)	Short-circuit protected		
Maximum voltage for $\overline{\text{ERROR}}$ pin		V_{IN}	
Maximum voltage for SENSE pin		V_{OUT}	
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) At elevated temperatures, devices must be derated based on package thermal resistance. The devices in TO-220 package must be derated at $R_{\theta JA}$ = 32°C/W (with 0.5 in^2, 1-oz. copper area), junction-to-ambient (with no heat sink). The devices in the TO-263 surface-mount package must be derated at $R_{\theta JA}$ = 40.3°C/W (with 0.5 in^2, 1-oz. copper area), junction-to-ambient. See *Application and Implementation* section.
(3) If used in a dual-supply system where the regulator load is returned to a negative supply, the output must be diode-clamped to ground.
(4) The output PMOS structure contains a diode between the IN and OUT terminals. This diode is normally reverse biased. This diode will get forward biased if the voltage at the output terminal is forced to be higher than the voltage at the input terminal. This diode can typically withstand 200 mA of DC current and 1 A of peak current.

8.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Input supply voltage (1)	2.5		7	V
Shutdown input voltage	−0.3		7	
Maximum operating current (DC)			1.5	A
Junction temperature	−40		125	°C

(1) The minimum operating value for V_{IN} is equal to either [$V_{OUT(NOM)}$ + $V_{DROPOUT}$] or 2.5 V, whichever is greater.

8.4 Thermal Information

THERMAL METRIC (1)		LP3852/LP3855			UNIT
		NDC	KTT	NDH	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance, High-K	65.2	40.3	32	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.2	43.4	43.8	
$R_{\theta JB}$	Junction-to-board thermal resistance	9.9	23.1	18.6	
ψ_{JT}	Junction-to-top characterization parameter	3.4	11.5	8.8	
ψ_{JB}	Junction-to-board characterization parameter	9.7	22	18	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	1	1.2	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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8.5 Electrical Characteristics

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1$ V, $I_{OUT} = 10$ mA, $C_{OUT} = 10$ µF, $V_{SD} = 2$ V, $T_J = 25°C$.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
V_{OUT}	Output voltage tolerance(3)	V_{OUT} +1 V ≤ V_{IN} ≤ 7 V 10 mA ≤ I_{OUT} ≤ 1.5 A	–1.5%	0	1.5%	
		For –40°C ≤ T_J ≤ 125°C	–3%		3%	
$\Delta V_{OUT}/\Delta V_{IN}$	Output voltage line regulation(3)	V_{OUT} +1 V ≤ V_{IN} ≤ 7 V		0.02%		
		For –40°C ≤ T_J ≤ 125°C		0.06%		
$\Delta V_{OUT}/\Delta I_{OUT}$	Output voltage load regulation(3)	10 mA ≤ I_{OUT} ≤ 1.5 A		0.06%		
		For –40°C ≤ T_J ≤ 125°C		0.12%		
V_{IN} - V_{OUT}	Dropout voltage TO-263 and TO-220(4)	I_{OUT} = 150 mA		24	35	mV
		For –40°C ≤ T_J ≤ 125°C			45	
		I_{OUT} = 1.5A		240	280	
		For –40°C ≤ T_J ≤ 125°C			380	
	Dropout voltage SOT(4), (5)	I_{OUT} = 150mA		26	35	
		For –40°C ≤ T_J ≤ 125°C			45	
		I_{OUT} = 1.5 A		260	320	
		For –40°C ≤ T_J ≤ 125°C			435	
I_{GND}	Ground pin current in normal operation mode	I_{OUT} = 150 mA		3	9	mA
		For –40°C ≤ T_J ≤ 125°C			10	
		I_{OUT} = 1.5 A		3	9	
		For –40°C ≤ T_J ≤ 125°C			10	
I_{GND}	Ground pin current in shutdown mode	V_{SD} ≤ 0.3V		0.01	10	µA
		-40°C ≤ T_J ≤ 85°C			50	
$I_{OUT(PK)}$	Peak output current	V_O ≥ $V_{O(NOM)}$ – 4%		1.8		A
SHORT CIRCUIT PROTECTION						
I_{SC}	Short circuit current			3.2		A
SHUTDOWN INPUT						
V_{SDT}	Shutdown threshold	V_{SDT} Rising from 0.3 V until Output = ON		1.3		V
		For –40°C ≤ T_J ≤ 125°C	2			
		V_{SDT} Falling from 2 V until Output = OFF		1.3		
		For –40°C ≤ T_J ≤ 125°C			0.3	
T_{dOFF}	Turnoff delay	I_{OUT} = 1.5 A		20		µs
T_{dON}	Turnon delay	I_{OUT} = 1.5 A		25		µs
I_{SD}	$\overline{SD}$ input current	V_{SD} = V_{IN}		1		nA
$\overline{ERROR}$ PIN						
V_T	Threshold	See(6)		10%		
		For –40°C ≤ T_J ≤ 125°C	5%		16%	
V_{TH}	Threshold hysteresis	See(6)		5%		
		For –40°C ≤ T_J ≤ 125°C	2%		8%	

(1) Limits are specified by testing, design, or statistical correlation.
(2) Typical numbers are at 25°C and represent the most likely parametric norm.
(3) Output voltage line regulation is defined as the change in output voltage from the nominal value due to change in the input line voltage. Output voltage load regulation is defined as the change in output voltage from the nominal value due to change in load current. The line and load regulation specification contains only the typical number. However, the limits for line and load regulation are included in the output voltage tolerance specification.
(4) Dropout voltage is defined as the minimum input to output differential voltage at which the output drops 2% below the nominal value. Dropout voltage specification applies only to output voltages of 2.5V and above. For output voltages below 2.5 V, the drop-out voltage is nothing but the input to output differential, since the minimum input voltage is 2.5 V.
(5) The SOT-223 package devices have slightly higher dropout due to increased bond wire resistance.
(6) $\overline{ERROR}$ threshold and hysteresis are specified as percentage of regulated output voltage. See *$\overline{ERROR}$ Flag Operation*.

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Electrical Characteristics (continued)

Unless otherwise specified: $V_{IN} = V_{OUT(NOM)} + 1$ V, $I_{OUT} = 10$ mA, $C_{OUT} = 10$ µF, $V_{SD} = 2$ V, $T_J = 25°C$.

PARAMETER		TEST CONDITIONS	MIN(1)	TYP(2)	MAX(1)	UNIT
$V_{EF(Sat)}$	$\overline{\text{ERROR}}$ pin saturation	$I_{sink} = 100$ µA		0.02		V
		For –40°C ≤ T_J ≤ 125°C			0.1	
Td	Flag reset delay			1		µs
I_{lk}	$\overline{\text{ERROR}}$ pin leakage current			1		nA
I_{max}	$\overline{\text{ERROR}}$ pin sink current	$V_{Error} = 0.5$ V		1		mA
AC PARAMETERS						
PSRR	Ripple rejection	$V_{IN} = V_{OUT} + 1$ V $C_{OUT} = 10$ µF $V_{OUT} = 3.3$V, f = 120 Hz		73		dB
		$V_{IN} = V_{OUT} + 0.5$ V $C_{OUT} = 10$ µF $V_{OUT} = 3.3$V, f = 120 Hz		57		
$\rho_{n(l/f)}$	Output noise density	f = 120 Hz		0.8		µV
e_n	Output noise voltage	BW = 10Hz – 100 kHz $V_{OUT} = 2.5$ V		150		µV (rms)
		BW = 300 Hz – 300 kHz $V_{OUT} = 2.5$ V		100		

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8.6 Typical Characteristics

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10 µF, C_{IN} = 10 µF, $\overline{SD}$ pin is tied to V_{IN}, V_{OUT} = 2.5 V, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 10 mA.

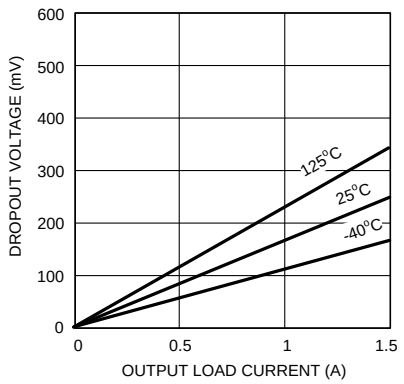
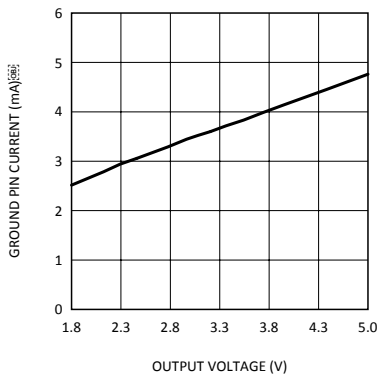


Figure 1. Dropout Voltage vs Output Load Current



I_{OUT} = 1.5 A

Figure 2. Ground Current vs Output Voltage

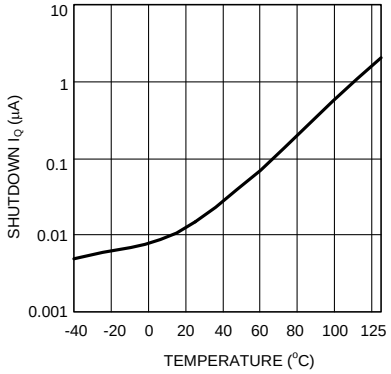


Figure 3. $\overline{SD}$ I_Q vs Junction Temperature

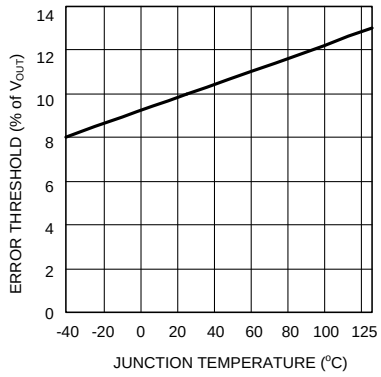


Figure 4. $\overline{ERROR}$ Threshold vs Junction Temperature

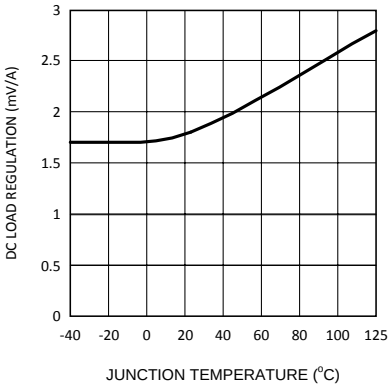


Figure 5. DC Load Reg. vs Junction Temperature

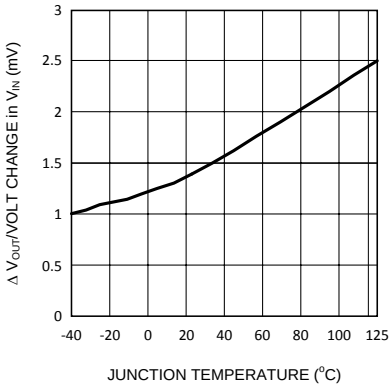


Figure 6. DC Line Regulation vs Temperature

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Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10 µF, C_{IN} = 10 µF, $\overline{SD}$ pin is tied to V_{IN}, V_{OUT} = 2.5 V, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 10 mA.

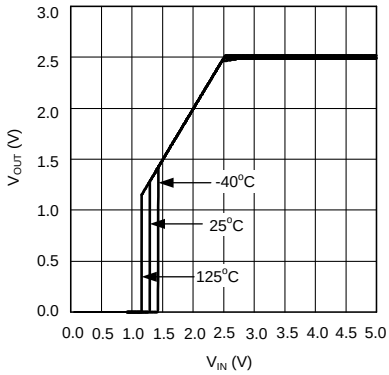


Figure 7. V_{IN} vs V_{OUT} Over Temperature

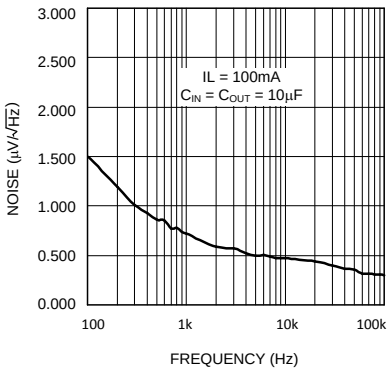
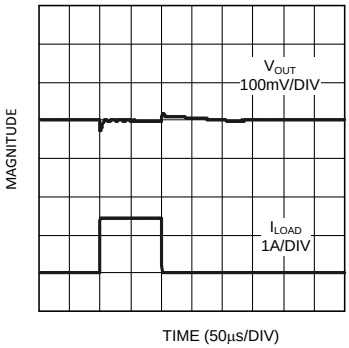
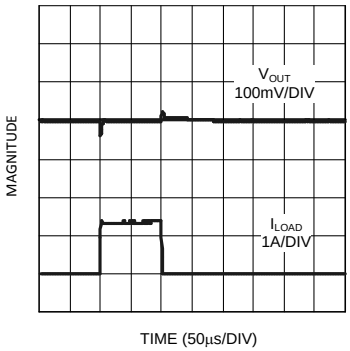


Figure 8. Noise vs Frequency



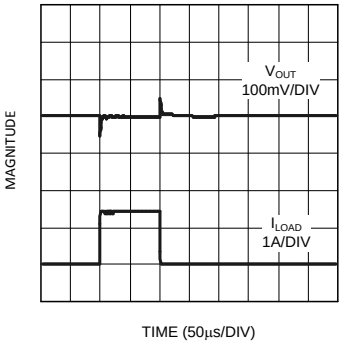
C_{IN} = C_{OUT} = 100 µF, OSCON

Figure 9. Load Transient Response



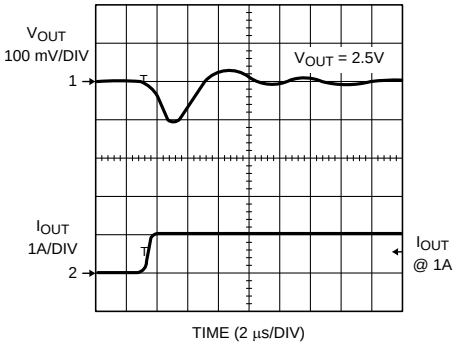
C_{IN} = C_{OUT} = 100 µF, POSCAP

Figure 10. Load Transient Response



C_{IN} = C_{OUT} = 100 µF, Tantalum

Figure 11. Load Transient Response

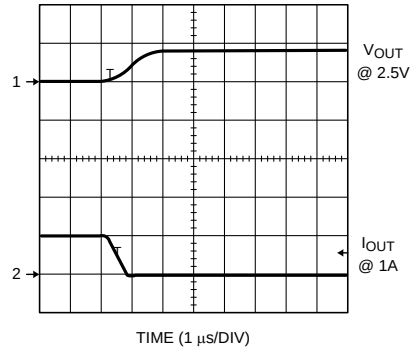


C_{IN} = 2 X 10 µF Ceramic
C_{OUT} = 2 X 10µF Ceramic

Figure 12. Load Transient Response

Typical Characteristics (continued)

Unless otherwise specified: T_J = 25°C, C_{OUT} = 10 µF, C_{IN} = 10 µF, $\overline{SD}$ pin is tied to V_{IN}, V_{OUT} = 2.5 V, V_{IN} = $V_{OUT(NOM)}$ + 1 V, I_{OUT} = 10 mA.



C_{IN} = 2 X 10 µF Ceramic
C_{OUT} = 2 X 10µF Ceramic

Figure 13. Load Transient Response

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9 Detailed Description

9.1 Overview

The LP3852 and LP3855 series of fast ultra-low dropout linear regulators operate from a 2.5-V to 7-V input supply. A wide range of preset output voltage options are available. These ultra-low dropout linear regulators respond very quickly to step changes in load, which makes them suitable for low voltage microprocessor applications. The LP3852 and LP3855 are developed on a CMOS process which allows low quiescent current operation independent of output load current. This CMOS process also allows the LP3852 and LP3855 to operate under extremely low dropout conditions.

9.2 Functional Block Diagrams

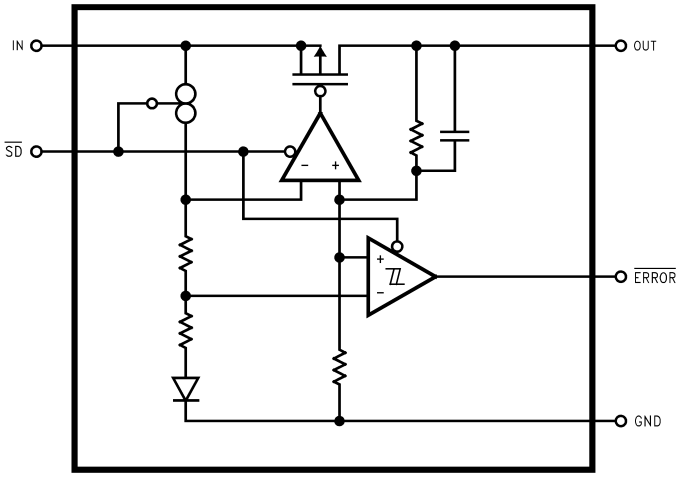

Figure 14. LP3852 Block Diagram

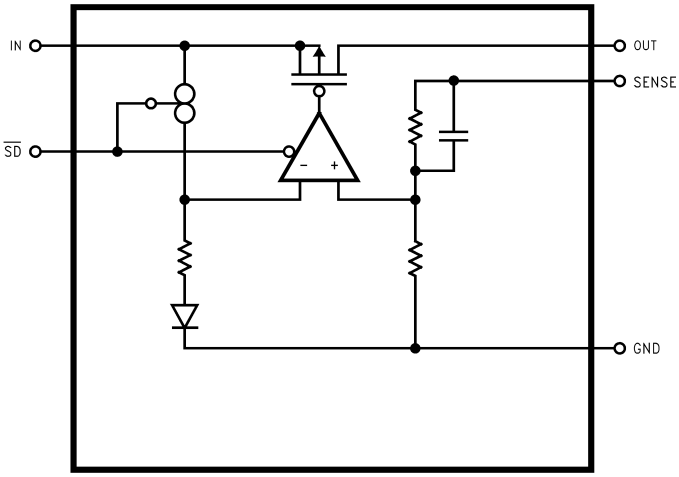

Figure 15. LP3855 Block Diagram

9.3 Feature Description

9.3.1 SENSE Pin

In applications where the regulator output is not very close to the load, LP3855 can provide better remote load regulation using the SENSE pin. Figure 16 depicts the advantage of the SENSE option. The LP3852 regulates the voltage at the OUT pin. Hence, the voltage at the remote load will be the regulator output voltage minus the drop across the trace resistance. For example, in the case of a 3.3-V output, if the trace resistance is 100 mΩ, the voltage at the remote load will be 3.15 V with 1.5 A of load current, I_{LOAD}. The LP3855 regulates the voltage at the SENSE pin. Connecting the SENSE pin to the remote load will provide regulation at the remote load, as shown in Figure 16. If the SENSE pin is not required, the SENSE pin must be connected to the OUT pin.

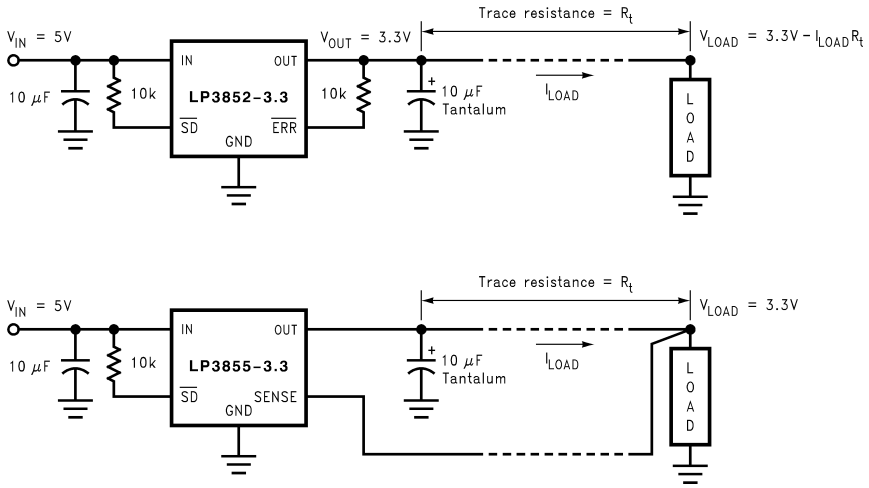

Figure 16. Improving Remote Load Regulation Using LP3855

9.3.2 $\overline{\text{SHUTDOWN}}$ ($\overline{\text{SD}}$) Operation

A CMOS Logic low level signal at the $\overline{\text{SD}}$ pin will turn off the regulator. $\overline{\text{SD}}$ must be actively terminated through a 10-kΩ pullup resistor for a proper operation. If this pin is driven from a source that actively pulls high and low (such as a CMOS rail-to-rail comparator), the pullup resistor is not required. This pin must be tied to V_{IN} if not used.

The $\overline{\text{SD}}$ pin threshold has no voltage hysteresis. If the $\overline{\text{SD}}$ pin is actively driven, the voltage transition must rise and fall cleanly and promptly.

9.3.3 Dropout Voltage

The dropout voltage of a regulator is defined as the minimum input-to-output differential required to stay within 2% of the nominal output voltage. For CMOS LDOs, the dropout voltage is the product of the load current and the $R_{ds(on)}$ of the internal MOSFET.

9.3.4 Reverse Current Path

The internal MOSFET in LP3852 and LP3855 has an inherent parasitic diode. During normal operation, the input voltage is higher than the output voltage and the parasitic diode is reverse biased. However, if the output is pulled above the input in an application, then current flows from the output to the input as the parasitic diode gets forward biased. The output can be pulled above the input as long as the current in the parasitic diode is limited to 200-mA continuous and 1-A peak.

9.3.5 Short-Circuit Protection

The LP3852 and LP3855 are short-circuit protected and in the event of a peak overcurrent condition, the short-circuit control loop will rapidly drive the output PMOS pass element off. Once the power pass element shuts down, the control loop will rapidly cycle the output on and off until the average power dissipation causes the thermal shutdown circuit to respond to servo the on/off cycling to a lower frequency. Please refer to for power dissipation calculations.

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Feature Description (continued)

9.3.6 $\overline{\text{ERROR}}$ Flag Operation

The LP3852 and LP3855 produce a logic low signal at the $\overline{\text{ERROR}}$ pin when the output drops out of regulation due to low input voltage, current limiting, or thermal limiting. This flag has a built in hysteresis. The timing diagram in Figure 17 shows the relationship between the $\overline{\text{ERROR}}$ flag and the output voltage. In this example, the input voltage is changed to demonstrate the functionality of the $\overline{\text{ERROR}}$ Flag.

The internal $\overline{\text{ERROR}}$ comparator has an open drain output stage; thus, the $\overline{\text{ERROR}}$ pin should be pulled high through a pullup resistor. Although the $\overline{\text{ERROR}}$ flag pin can sink current of 1 mA, this current is energy drain from the input supply. Hence, the value of the pullup resistor should be in the range of 10 kΩ to 1 MΩ. *The $\overline{\text{ERROR}}$ pin must be connected to ground if this function is not used.* It should also be noted that when the shutdown pin is pulled low, the $\overline{\text{ERROR}}$ pin is forced to be invalid for reasons of saving power in shutdown mode.

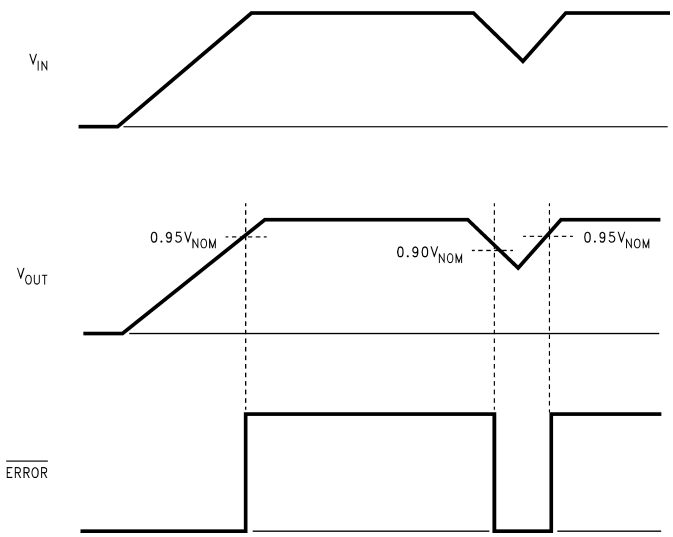

Figure 17. $\overline{\text{ERROR}}$ Operation

9.4 Device Functional Modes

9.4.1 Operation with $V_{OUT(TARGET)}$ + 0.1 V ≤ V_{IN} ≤ 7 V

The device operate if the input voltage is equal to, or exceeds $V_{OUT(TARGET)}$ + 0.1 V. At input voltages below the minimum V_{IN} requirement, the devices do not operate correctly and output voltage may not reach target value.

9.4.2 Operation With $\overline{\text{SD}}$ Pin Control

A CMOS Logic low level signal at the $\overline{\text{SD}}$ pin will turn off the regulator. The $\overline{\text{SD}}$ pin must be actively terminated through a 10-kΩ pullup resistor for a proper operation.

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The LP3852 and LP3855 devices can provide 1.5-A output current with 2.5-V to 7-V input. A minimum 10-uF output capacitor is required for loop stability. An input capacitor of at least 10 µF is required . Pin $\overline{SD}$ must be tied to input if not used. For LP3852, $\overline{ERROR}$ pin should be pulled high through a pullup resistor. For LP3855, if the sense option is not required , the SENSE pin must be connected to the OUT pin.

10.2 Typical Applications

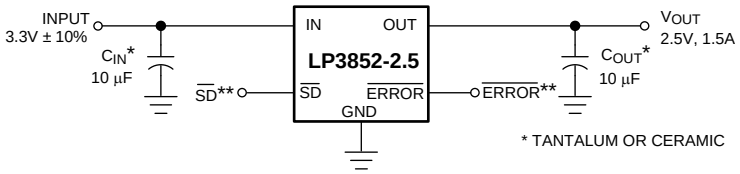

Figure 18. LP3852 Typical Application

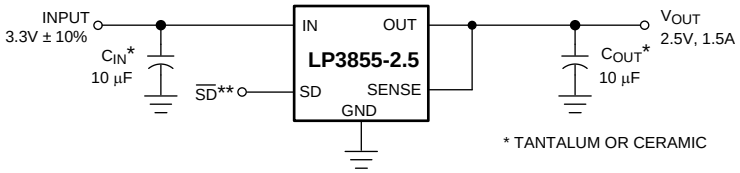

Figure 19. LP3855 Typical Application

10.2.1 Design Requirements

DESIGN PARAMETERS	VALUE
Input voltage	3.3 V, ±10%
Output voltage	2.5 V, ±3%
Output current	1.5 A (maximum)
Input capacitor	10 µF (minimum)
Output capacitor	10 µF (minimum)
$\overline{ERROR}$ pullup resistor (LP3852 only)	10 kΩ

10.2.2 Detailed Design Procedure

10.2.2.1 External Capacitors

Like any low dropout regulator, external capacitors are required to assure stability. These capacitors must be correctly selected for proper performance.

10.2.2.1.1 Input Capacitor

An input capacitor of at least 10 µF is required. Ceramic or tantalum may be used, and capacitance may be increased without limit.

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10.2.2.1.2 Output Capacitor

An output capacitor is required for loop stability. It must be located less than 1 cm from the device and connected directly to the output and ground pins using traces which have no other currents flowing through them (see *Layout Guidelines*).

The minimum amount of output capacitance that can be used for stable operation is 10 µF. For general usage across all load currents and operating conditions, the part was characterized using a 10-µF tantalum input capacitor. The minimum and maximum stable equivalent series resistance (ESR) range for the output capacitor was then measured which kept the device stable, assuming any output capacitor whose value is greater than 10 µF (see Figure 20).

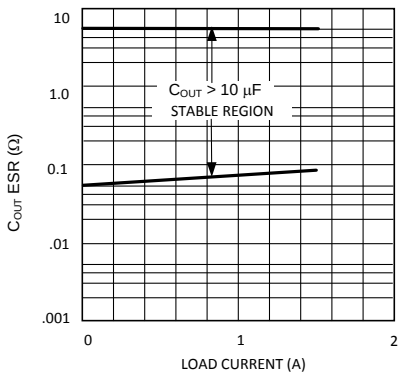

Figure 20. ESR Curve For C_{OUT} (with 10-µF Tantalum Input Capacitor)

It should be noted that it is possible to operate the part with an output capacitor whose ESR is below these limits, assuming that sufficient ceramic input capacitance is provided. This will allow stable operation using ceramic output capacitors (see *Operation with Ceramic Output Capacitors*).

10.2.2.2 Operation with Ceramic Output Capacitors

LP385X voltage regulators can operate with ceramic output capacitors if the values of the input and output capacitors are selected appropriately. The total ceramic output capacitance must be equal to or less than a specified maximum value in order for the regulator to remain stable over all operating conditions. This maximum amount of ceramic output capacitance is dependent upon the amount of ceramic input capacitance used as well as the load current of the application. This relationship is shown in Figure 21, which graphs the maximum stable value of ceramic output capacitance as a function of ceramic input capacitance for load currents of 1.5 A.

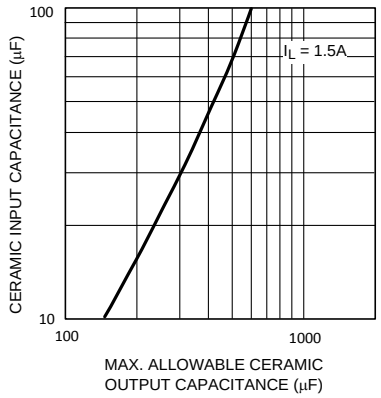

Figure 21. Maximum Ceramic Output Capacitance vs Ceramic Input Capacitance

If the maximum load current is 1.5 A and a 10-µF ceramic input capacitor is used, the regulator will be stable with ceramic output capacitor values from 10 µF up to about 150 µF. When calculating the total ceramic output capacitance present in an application, it is necessary to include any ceramic bypass capacitors connected to the regulator output.

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10.2.2.3 Selecting A Capacitor

It is important to note that capacitance tolerance and variation with temperature must be taken into consideration when selecting a capacitor so that the minimum required amount of capacitance is provided over the full operating temperature range. In general, a good tantalum capacitor will show very little capacitance variation with temperature, but a ceramic may not be as good (depending on dielectric type). Aluminum electrolytics also typically have large temperature variation of capacitance value.

Equally important to consider is a capacitor's ESR change with temperature: this is not an issue with ceramics, as their ESR is extremely low. However, it is very important in Tantalum and aluminum electrolytic capacitors. Both show increasing ESR at colder temperatures, but the increase in aluminum electrolytic capacitors is so severe they may not be feasible for some applications (see *Capacitor Characteristics*).

10.2.2.4 Capacitor Characteristics

10.2.2.4.1 Ceramic

For values of capacitance in the 10-µF to 100-µF range, ceramics are usually larger and more costly than tantalums but give superior AC performance for bypassing high frequency noise because of very low ESR (typically less than 10 mΩ). However, some dielectric types do not have good capacitance characteristics as a function of voltage and temperature.

Z5U and Y5V dielectric ceramics have capacitance that drops severely with applied voltage. A typical Z5U or Y5V capacitor can lose 60% of its rated capacitance with half of the rated voltage applied to it. The Z5U and Y5V also exhibit a severe temperature effect, losing more than 50% of nominal capacitance at high and low limits of the temperature range.

X7R and X5R dielectric ceramic capacitors are strongly recommended if ceramics are used, as they typically maintain a capacitance range within ±20% of nominal over full operating ratings of temperature and voltage. Of course, they are typically larger and more costly than Z5U/Y5U types for a given voltage and capacitance.

10.2.2.4.2 Tantalum

Solid tantalum capacitors are typically recommended for use on the output because their ESR is very close to the ideal value required for loop compensation.

Tantalum capacitors also have good temperature stability: a good quality tantalum capacitor will typically show a capacitance value that varies less than 10-15% across the full temperature range of 125°C to −40°C. ESR will vary only about 2X going from the high to low temperature limits.

The increasing ESR at lower temperatures can cause oscillations when marginal quality capacitors are used (if the ESR of the capacitor is near the upper limit of the stability range at room temperature).

10.2.2.4.3 Aluminum

This capacitor type offers the most capacitance for the money. The disadvantages are that they are larger in physical size, not widely available in surface mount, and have poor AC performance (especially at higher frequencies) due to higher ESR and ESL.

Compared by size, the ESR of an aluminum electrolytic is higher than either tantalum or ceramic, and it also varies greatly with temperature. A typical aluminum electrolytic can exhibit an ESR increase of as much as 50X when going from 25°C down to −40°C.

It should also be noted that many aluminum electrolytics only specify impedance at a frequency of 120 Hz, which indicates they have poor high frequency performance. Only aluminum electrolytics that have an impedance specified at a higher frequency (between 20 kHz and 100 kHz) should be used for the LP385X. Derating must be applied to the manufacturer's ESR specification, since it is typically only valid at room temperature.

Any applications using aluminum electrolytics should be thoroughly tested at the lowest ambient operating temperature where ESR is maximum.

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10.2.2.5 Turnon Characteristics For Output Voltages Programmed to 2 V or Below

As V_{IN} increases during start-up, the regulator output will track the input until V_{IN} reaches the minimum operating voltage (typically about 2.2 V). For output voltages programmed to 2 V or below, the regulator output may momentarily exceed its programmed output voltage during start up. Outputs programmed to voltages above 2 V are not affected by this behavior.

10.2.2.6 Output Noise

Noise is specified in two ways:

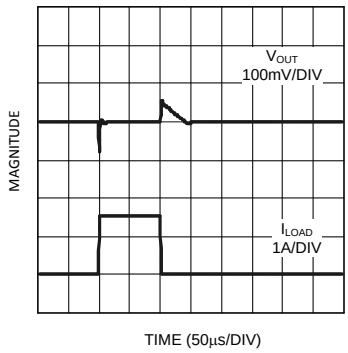
- *Spot Noise* or *Output Noise Density* is the RMS sum of all noise sources, measured at the regulator output, at a specific frequency (measured with a 1-Hz bandwidth). This type of noise is usually plotted on a curve as a function of frequency.
- *Total Output Noise* or *Broad-Band Noise* is the RMS sum of spot noise over a specified bandwidth, usually several decades of frequencies.

Attention should be paid to the units of measurement. Spot noise is measured in units µV/√Hz or nV/√Hz, and total output noise is measured in μV_{RMS}.

The primary source of noise in low-dropout regulators is the internal reference. In CMOS regulators, noise has a low frequency component and a high frequency component, which depend strongly on the silicon area and quiescent current. Noise can be reduced in two ways: by increasing the transistor area or by increasing the current drawn by the internal reference. Increasing the area will decrease the chance of fitting the die into a smaller package. Increasing the current drawn by the internal reference increases the total supply current (ground pin current). Using an optimized trade-off of ground pin current and die size, LP3852 and LP3855 achieve low noise performance and low quiescent-current operation.

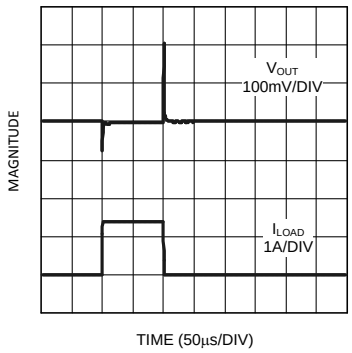
The total output noise specification for LP3852 and LP3855 is presented in the *Electrical Characteristics* table. The Output noise density at different frequencies is represented by a curve under *Typical Characteristics*.

10.2.3 Application Curves



$C_{IN} = C_{OUT}$ = 10 µF, OSCON

Figure 22. Load Transient Response



$C_{IN} = C_{OUT}$ = 10 µF, Tantalum

Figure 23. Load Transient Response

11 Power Supply Recommendations

The LP3852 and LP3855 devices are designed to operate from an input voltage supply range between 2.5 V and 7 V. The input voltage range provides adequate headroom in order for the device to have a regulated output. This input supply must be well regulated. An input capacitor of at least 10 µF is required.

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12 Layout

12.1 Layout Guidelines

Good PC layout practices must be used or instability can be induced because of ground loops and voltage drops. The input and output capacitors must be directly connected to the IN, OUT, and ground pins of the regulator using traces which do not have other currents flowing in them (Kelvin connect).

The best way to do this is to lay out C_{IN} and C_{OUT} near the device with short traces to the IN, OUT, and ground pins. The regulator ground pin should be connected to the external circuit ground so that the regulator and its capacitors have a "single point ground".

It should be noted that stability problems have been seen in applications where "vias" to an internal ground plane were used at the ground points of the IC and the input and output capacitors. This was caused by varying ground potentials at these nodes resulting from current flowing through the ground plane. Using a single point ground technique for the regulator and its capacitors fixed the problem.

Since high current flows through the traces going into IN and coming from OUT, Kelvin connect the capacitor leads to these pins so there is no voltage drop in series with the input and output capacitors.

12.2 Layout Example

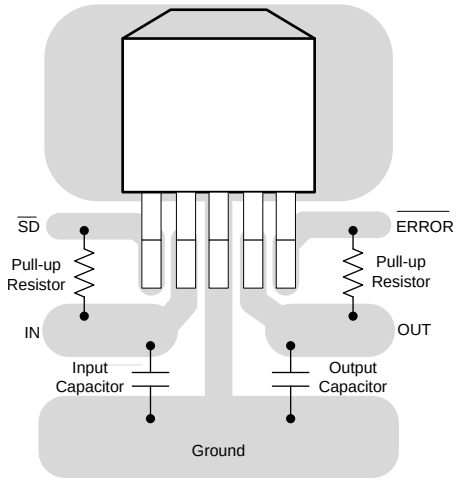

Figure 24. LP3852 TO-263 Package Typical Layout

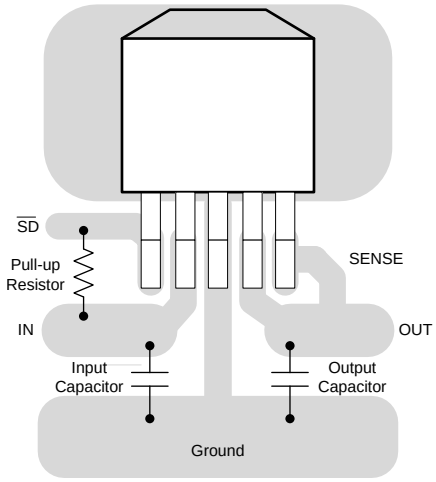

Figure 25. LP3855 TO-263 Package Typical Layout

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12.3 RFI and/or EMI Susceptibility

Radio frequency interference (RFI) and electromagnetic interference (EMI) can degrade any integrated circuit performance because of the small dimensions of the geometries inside the device. In applications where circuit sources are present which generate signals with significant high frequency energy content (> 1 MHz), care must be taken to ensure that this does not affect the device regulator.

If RFI and/or EMI noise is present on the input side of the regulator (such as applications where the input source comes from the output of a switching regulator), good ceramic bypass capacitors must be used at the IN pin of the device.

If a load is connected to the device output which switches at high speed (such as a clock), the high-frequency current pulses required by the load must be supplied by the capacitors on the device output. Since the bandwidth of the regulator loop is less than 100 kHz, the control circuitry cannot respond to load changes above that frequency. This means the effective output impedance of the device at frequencies above 100 kHz is determined only by the output capacitor or capacitors.

In applications where the load is switching at high speed, the output of the IC may need RF isolation from the load. It is recommended that some inductance be placed between the output capacitor and the load, and good RF bypass capacitors be placed directly across the load.

PCB layout is also critical in high noise environments, since RFI and/or EMI is easily radiated directly into PC traces. Noisy circuitry should be isolated from "clean" circuits where possible, and grounded through a separate path. At MHz frequencies, ground planes begin to look inductive and RFI and/or EMI can cause ground bounce across the ground plane.

In multi-layer PCB applications, care should be taken in layout so that noisy power and ground planes do not radiate directly into adjacent layers which carry analog power and ground.

12.4 Power Dissipation/Heatsinking

The LP3852 and LP3855 can deliver a continuous current of 1.5 A over the full operating temperature range. A heatsink may be required depending on the maximum power dissipation and maximum ambient temperature of the application. Under all possible conditions, the junction temperature must be within the range specified under operating conditions. The total power dissipation of the device is given by:

$$P_D = (V_{IN} - V_{OUT})I_{OUT} + (V_{IN})I_{GND}$$

where

- I_{GND} is the operating ground current of the device (specified under *Electrical Characteristics*). (1)

The maximum allowable temperature rise (T_{Rmax}) depends on the maximum ambient temperature (T_{Amax}) of the application, and the maximum allowable junction temperature (T_{Jmax}):

$$T_{Rmax} = T_{Jmax} - T_{Amax} \quad (2)$$

The maximum allowable value for junction to ambient thermal resistance, $R_{\theta JA}$, can be calculated using the formula:

$$R_{\theta JA} = T_{Rmax} / P_D \quad (3)$$

The LP3852 and LP3855 are available in TO-220 and TO-263 packages. The thermal resistance depends on amount of copper area or heat sink, and on air flow. If the maximum allowable value of $R_{\theta JA}$ calculated in Equation 3 is ≥ 60 °C/W for TO-220 package and ≥ 60°C/W for TO-263 package, no heatsink is needed since the package can dissipate enough heat to satisfy these requirements. If the value for allowable $R_{\theta JA}$ falls below these limits, a heat sink is required.

12.4.1 Heatsinking TO-220 Package

The thermal resistance of a TO-220 package can be reduced by attaching it to a heat sink or a copper plane on a PC board. If a copper plane is to be used, the values of $R_{\theta JA}$ will be same as shown in next section for TO-263 package.

The heatsink to be used in the application should have a heatsink to ambient thermal resistance,

$$R_{\theta HA} \leq R_{\theta JA} - R_{\theta CH} - R_{\theta JC}.$$

Power Dissipation/Heatsinking (continued)

In this equation, $R_{\theta CH}$ is the thermal resistance from the case to the surface of the heat sink, and $R_{\theta JC}$ is the thermal resistance from the junction to the surface of the case. $R_{\theta JC}$ is about 3°C/W for a TO-220 package. The value for $R_{\theta CH}$ depends on method of attachment, insulator, etc. $R_{\theta CH}$ varies between 1.5°C/W to 2.5°C/W. If the exact value is unknown, 2°C/W can be assumed.

12.4.2 Heatsinking TO-263 Package

The TO-263 package uses the copper plane on the PCB as a heatsink. The tab of these packages are soldered to the copper plane for heat sinking. Figure 26 shows a curve for the $R_{\theta JA}$ of TO-263 package for different copper area sizes, using a typical PCB with 1 ounce copper and no solder mask over the copper area for heat sinking.

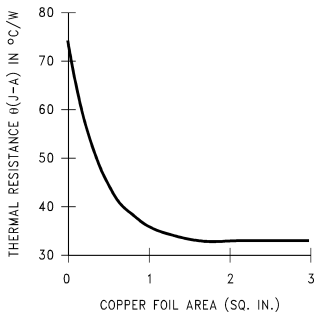

Figure 26. $R_{\theta JA}$ vs Copper (1 Ounce) Area for TO-263 package

As shown in the figure, increasing the copper area beyond 1 square inch produces very little improvement. The minimum value for $R_{\theta JA}$ for the TO-263 package mounted to a PCB is 32°C/W.

Figure 27 shows the maximum allowable power dissipation for TO-263 packages for different ambient temperatures, assuming $R_{\theta JA}$ is 35°C/W and the maximum junction temperature is 125°C.

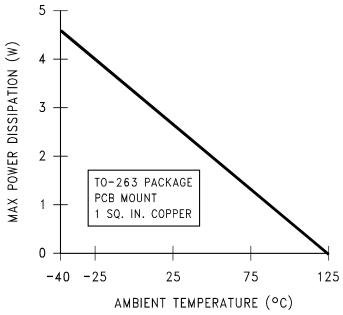

Figure 27. Maximum Power Dissipation vs Ambient Temperature for TO-263 Package

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13 Device and Documentation Support

13.1 Related Links

Table 1 lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
LP3852	Click here	Click here	Click here	Click here	Click here
LP3855	Click here	Click here	Click here	Click here	Click here

13.2 Trademarks

All trademarks are the property of their respective owners.

13.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3852EMP-1.8	NRND	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHTB	
LP3852EMP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHTB	Samples
LP3852EMP-2.5	NRND	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHUB	
LP3852EMP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHUB	Samples
LP3852EMP-3.3	NRND	SOT-223	NDC	5	1000	TBD	Call TI	Call TI	-40 to 125	LHVB	
LP3852EMP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHVB	Samples
LP3852EMP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHXB	Samples
LP3852EMPX-1.8/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHTB	Samples
LP3852ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3852ES -1.8	Samples
LP3852ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3852ES -2.5	Samples
LP3852ES-3.3	NRND	DDPAK/ TO-263	KTT	5	45	TBD	Call TI	Call TI	-40 to 125	LP3852ES -3.3	
LP3852ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3852ES -3.3	Samples
LP3852ES-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3852ES -5.0	Samples
LP3852ESX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3852ES -1.8	Samples
LP3852ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3852ES -2.5	Samples
LP3852ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3852ES -3.3	Samples
LP3852ESX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3852ES -5.0	Samples
LP3852ET-1.8/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3852ET -1.8	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3852ET-2.5/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3852ET -2.5	Samples
LP3852ET-3.3/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3852ET -3.3	Samples
LP3852ET-5.0/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3852ET -5.0	Samples
LP3855EMP-1.8/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHYB	Samples
LP3855EMP-2.5/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LHZB	Samples
LP3855EMP-3.3/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJ1B	Samples
LP3855EMP-5.0/NOPB	ACTIVE	SOT-223	NDC	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJ2B	Samples
LP3855EMPX-5.0/NOPB	ACTIVE	SOT-223	NDC	5	2000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	LJ2B	Samples
LP3855ES-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3855ES -1.8	Samples
LP3855ES-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3855ES -2.5	Samples
LP3855ES-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3855ES -3.3	Samples
LP3855ES-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	45	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3855ES -5.0	Samples
LP3855ESX-1.8/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3855ES -1.8	Samples
LP3855ESX-2.5/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3855ES -2.5	Samples
LP3855ESX-3.3/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3855ES -3.3	Samples
LP3855ESX-5.0/NOPB	ACTIVE	DDPAK/ TO-263	KTT	5	500	Pb-Free (RoHS Exempt)	CU SN	Level-3-245C-168 HR	-40 to 125	LP3855ES -5.0	Samples
LP3855ET-1.8/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3855ET -1.8	Samples
LP3855ET-3.3/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3855ET -3.3	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LP3855ET-5.0/NOPB	ACTIVE	TO-220	NDH	5	45	Green (RoHS & no Sb/Br)	CU SN	Level-1-NA-UNLIM	-40 to 125	LP3855ET -5.0	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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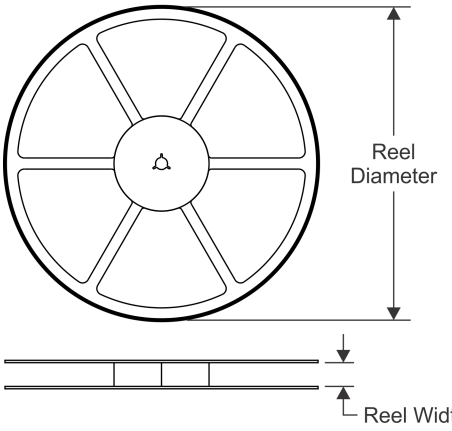
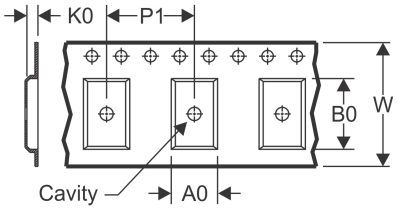
TAPE AND REEL INFORMATION

REEL DIMENSIONS

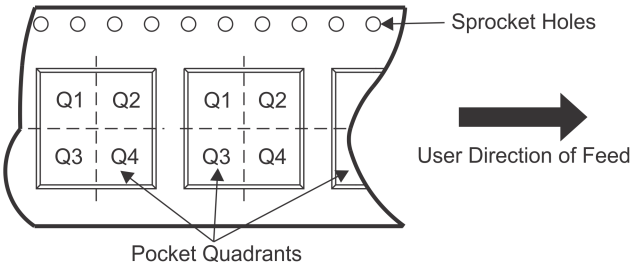


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

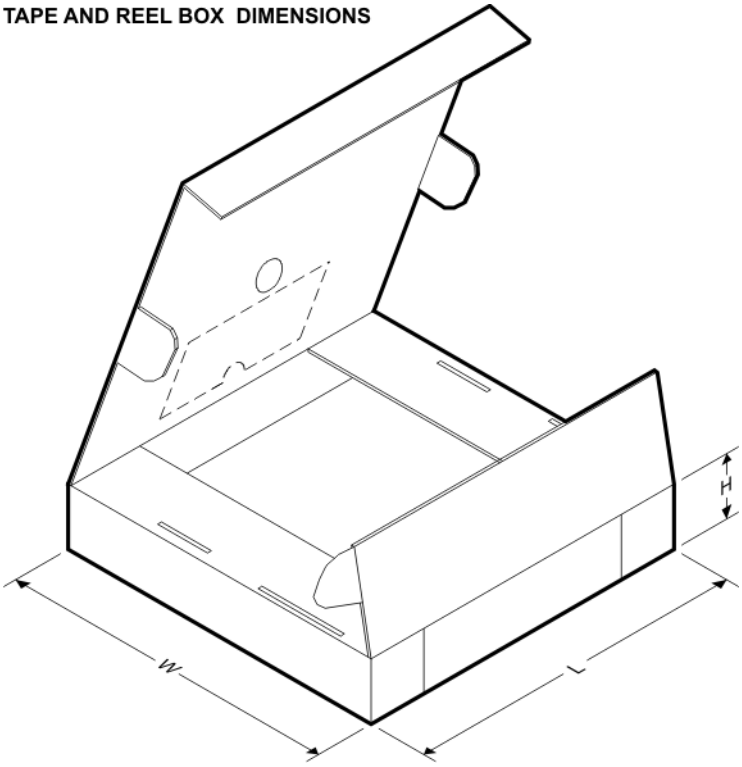


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3852EMP-1.8	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3852EMP-1.8/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3852EMP-2.5	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3852EMP-2.5/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3852EMP-3.3	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3852EMP-3.3/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3852EMP-5.0/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3852EMPX-1.8/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3852ESX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3852ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3852ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3852ESX-5.0/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3855EMP-1.8/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3855EMP-2.5/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3855EMP-3.3/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LP3855EMP-5.0/NOPB	SOT-223	NDC	5	1000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3855EMPX-5.0/NOPB	SOT-223	NDC	5	2000	330.0	16.4	7.0	7.5	2.2	12.0	16.0	Q3
LP3855ESX-1.8/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3855ESX-2.5/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3855ESX-3.3/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2
LP3855ESX-5.0/NOPB	DDPAK/ TO-263	KTT	5	500	330.0	24.4	10.75	14.85	5.0	16.0	24.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3852EMP-1.8	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3852EMP-1.8/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3852EMP-2.5	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3852EMP-2.5/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3852EMP-3.3	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3852EMP-3.3/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3852EMP-5.0/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3852EMPX-1.8/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LP3852ESX-1.8/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3852ESX-2.5/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3852ESX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3852ESX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3855EMP-1.8/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3855EMP-2.5/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3855EMP-3.3/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3855EMP-5.0/NOPB	SOT-223	NDC	5	1000	367.0	367.0	35.0
LP3855EMPX-5.0/NOPB	SOT-223	NDC	5	2000	367.0	367.0	35.0
LP3855ESX-1.8/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3855ESX-2.5/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3855ESX-3.3/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0
LP3855ESX-5.0/NOPB	DDPAK/TO-263	KTT	5	500	367.0	367.0	45.0

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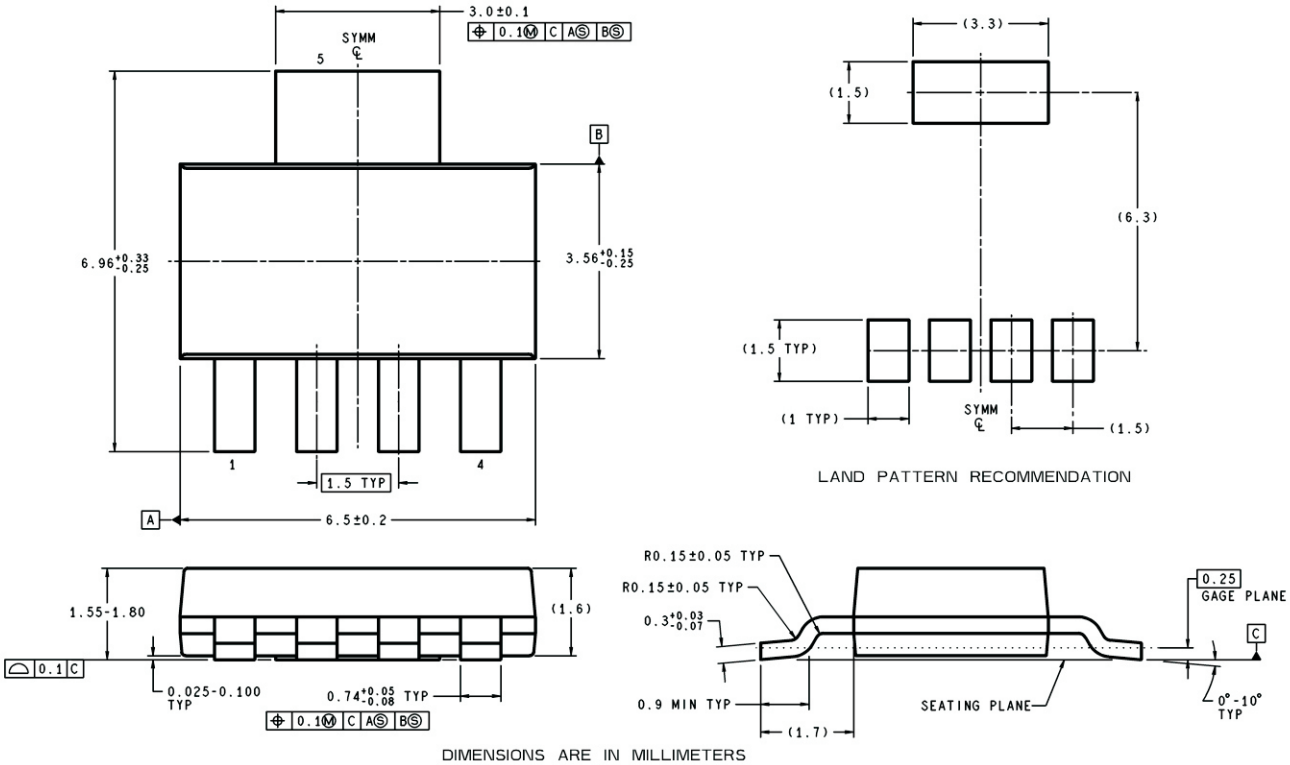
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B
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4
1.5 TYP
A
6.5±0.2
(3.3)
(1.5)
(6.3)
(1.5 TYP)
(1 TYP)
SYMM
(1.5)
LAND PATTERN RECOMMENDATION
1.55-1.80
(1.6)
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0.025-0.100 TYP
0.74 +0.05 -0.08 TYP
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R0.15±0.05 TYP
R0.15±0.05 TYP
0.3 +0.03 -0.07
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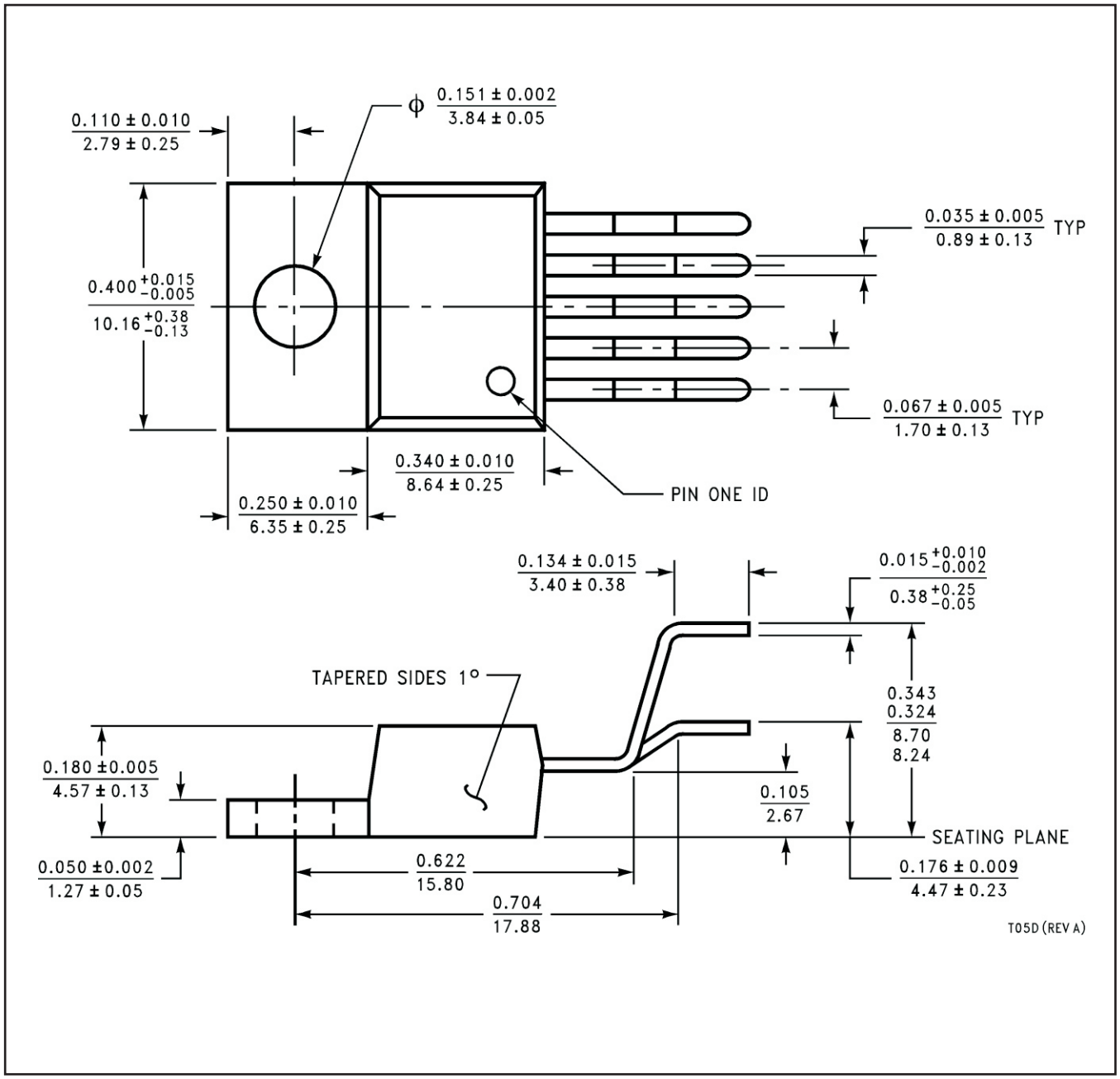
MP05A (Rev A)

NDH0005D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ϕ 0.151 ± 0.002
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0.89 ± 0.13
TYP
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10.16 +0.38 −0.13
0.067 ± 0.005
1.70 ± 0.13
TYP
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PIN ONE ID
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0.38 +0.25 −0.05
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8.24
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2.67
SEATING PLANE
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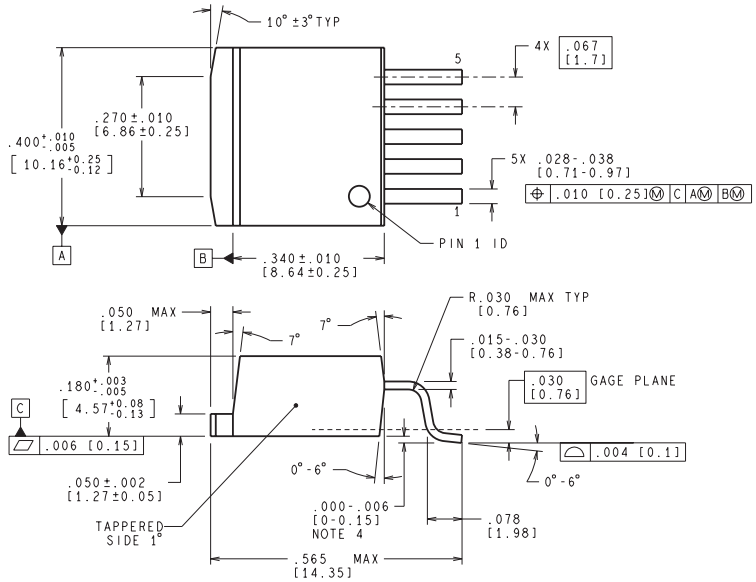
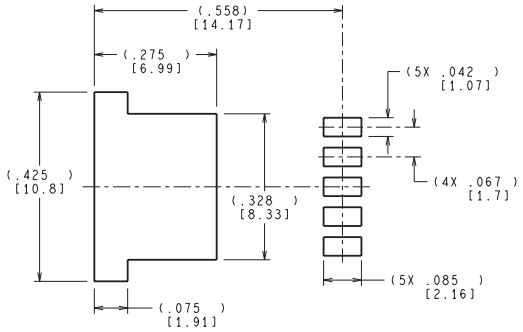
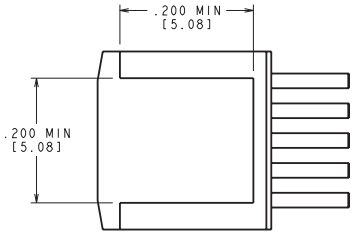
KTT0005B





LAND PATTERN RECOMMENDATION



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TS5B (Rev D)

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Designer will fully indemnify TI and its representatives against any damages, costs, losses, and/or liabilities arising out of Designer's non-compliance with the terms and provisions of this Notice.

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